Matter No.: 01997-254003

Applicant(s): Arvind Mithal et al.

DIGITAL CIRCUIT SYNTHESIS SYSTEM

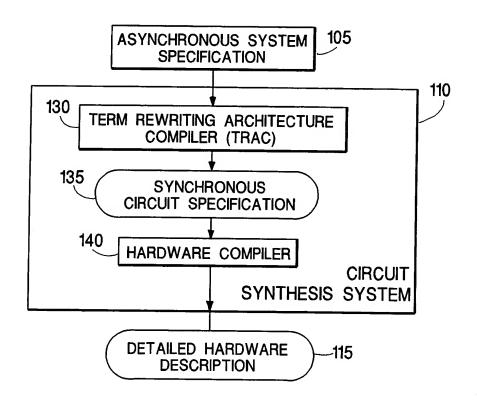


FIG. 1

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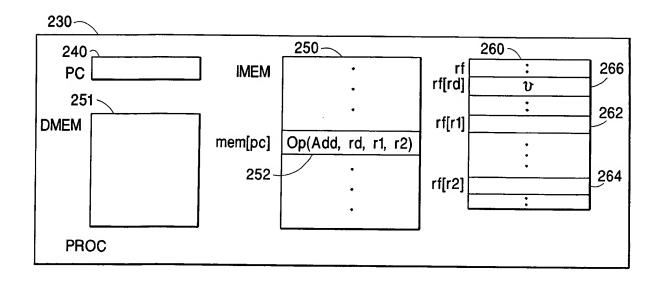


FIG. 2A

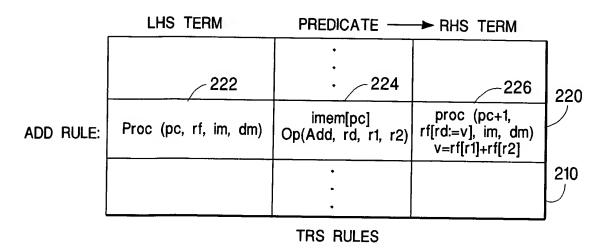


FIG. 2B

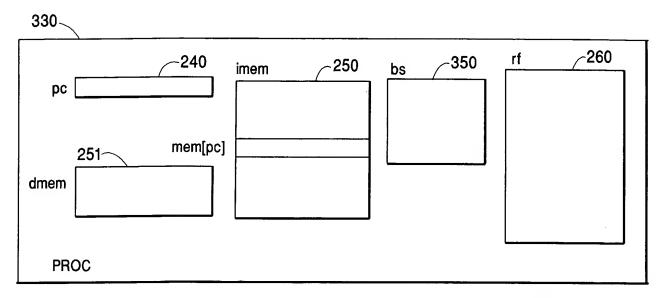
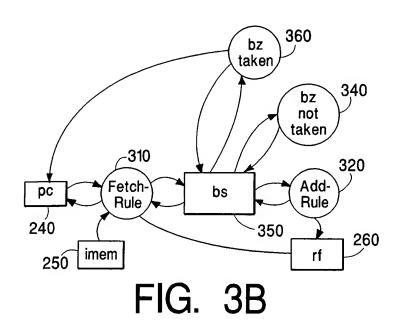
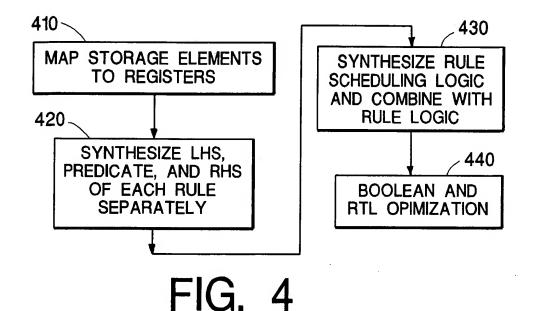
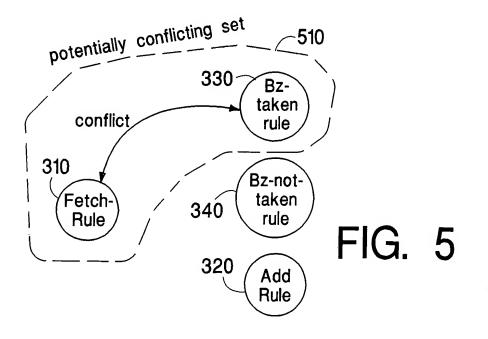


FIG. 3A

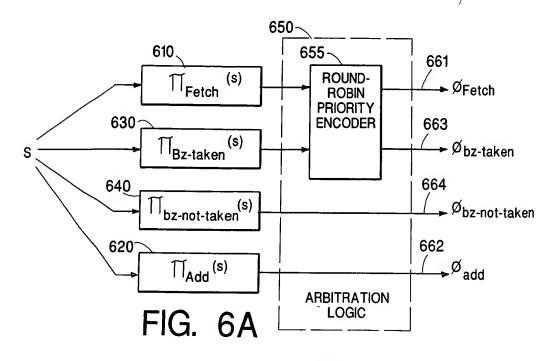






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DIGITAL CÍRCUIT SYNTHESIS SYSTEM



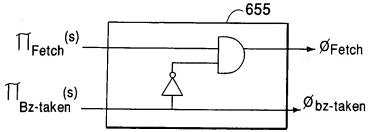
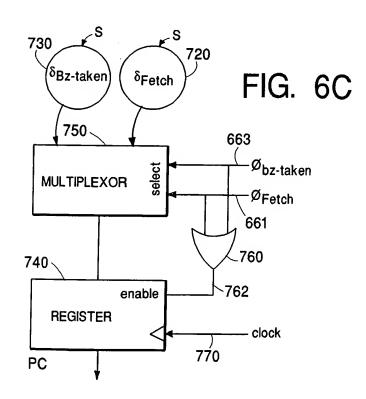


FIG. 6B

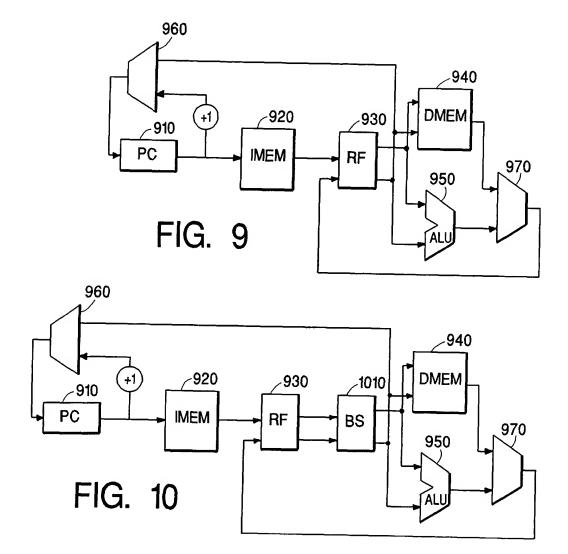


DIGITAL CIRCUIT SYNTHESIS SYSTEM

```
701 Type
             PROC = Proc(PC,RF,IMEM,DMEM)
702 Type
                PC = Bit[n]
703 Type
             ADDR = Bit[n]
704 Type
            VALUE = Bit[n]
                RF = Array VALUE[RNAME]
705 Type
706 Type
           RNAME = Reg0 \parallel Reg1 \parallel Reg2 \parallel Reg3 \parallel .... Regm
707 Type
             IMEM = Array INST[PC]
            DMEM = Array VALUE[ADDR]
708 Type
709 Type
             INST = Loadc(RNAME, VALUE)
                   || Loadpc(RNAME)
710
                   || Op(MINOR,RNAME,RNAME,RNAME)
711
                   || Bz(RNAME, RNAME)
712
                   || Load(RNAME,RNAME)
713
                   || Store(RNAME,RNAME)
714
715 Type
           MINOR = Add || Sub || \dots
                                            FIG. 7
```

```
801 Proc(pc,rf,im,dm)
802 if im[pc] \equiv Loadc(rd, const)
                                                Proc(pc+1,rf[rd:=const],im,dm)
803 if im[pc] \equiv Loadpc(rd)
                                                Proc(pc+1,rf[rd:=pc],im,dm)
804 if im[pc] \equiv Op(op,rd,r1,r2)
                                                Proc(pc+1,rf[rd:=op(rf[r1],rf[r2])],im,dm)
                                                 Proc(rf[rt],rf,im,dm)
805 if im[pc] \equiv Bz(rc,rt) \& rf[rc] \equiv 0
                                           \rightarrow
806 if im[pc] \equiv Bz(rc,rt) \& rf[rc] \neq 0
                                                 Proc(pc+1,rf,im,dm)
                                                 Proc(pc+1,rf[rd:=dm[rf[ra]]),im,dm)
807 if im[pc]≡Load(rd,ra)
808 if im[pc] \equiv Store(ra,r)
                                                 Proc(pc+1,rf,im,dm[rf[ra]:=rf[r]])
```

FIG. 8



DIGITAL CIRCUIT SYNTHESIS SYSTEM

```
1101 Type PROC<sub>p</sub> = Proc<sub>p</sub>(PC,RF,BS,IMEM,DMEM)

1102 Type BS = FIFO ITEMP

1103 Type ITEMP = Op(MINOR,RNAME,VALUE,VALUE)

1104 || Bz(VALUE,VALUE)

1105 || Load(RNAME,ADDR)

1106 || Store(ADDR.VALUE) FIG. 11
```

```
Proc<sub>p</sub>(pc,rf,bs,im,dm)

1202

if im[pc] \equiv inst and (Source(inst) \cap Target(bs) \equiv \empty)

1203 \to \text{Proc}_p(pc+1,rf,enq(bs,Decode(inst)),im,dm)}

FIG. 12A
```

```
1211 \operatorname{Proc}_{p}(pc,rf,bs,im,dm) where \operatorname{itemp:=first}(bs)

1212 \operatorname{if} \operatorname{itemp\equiv Op}(op,rd,v1,v2) \rightarrow \operatorname{Proc}_{p}(pc,rf[rd:=op(v1,v2)],\operatorname{deq}(bs),im,dm)

1213 \operatorname{if} \operatorname{itemp\equiv Bz}(vc,vt) & vc\equiv 0 \rightarrow \operatorname{Proc}_{p}(vt,rf,\operatorname{clear}(\overline{bs}),im,dm)

1214 \operatorname{if} \operatorname{itemp\equiv Bz}(vc,vt) & vc\neq 0 \rightarrow \operatorname{Proc}_{p}(pc,rf,\operatorname{deq}(bs),im,dm)

1215 \operatorname{if} \operatorname{itemp\equiv Load}(rd,va) \rightarrow \operatorname{Proc}_{p}(pc,rf[rd:=dm[va]],\operatorname{deq}(bs),im,dm)

1216 \operatorname{if} \operatorname{itemp\equiv Store}(va,v) \rightarrow \operatorname{Proc}_{p}(pc,rf,\operatorname{deq}(bs),im,dm[va:=v])
```

FIG. 12B

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 $\mathsf{Proc}_p(\mathit{pc},(\mathit{rf}[\mathit{rd}{:=} op(v\mathit{I},\mathit{v2})])[\mathit{rd}{:=} op'(v\mathit{I}',\mathit{v2}')],\mathsf{deq}(\mathsf{deq}(\mathit{bs})),\mathit{im},\mathit{dm})$

 $Proc_p(pc, rf, bs, im, dm)$ where Op(op, rd, v1, v2):=first(bs), itemp:=first(deq(bs))

1312 if itemp≡Op(op',rd',v1',v2') 1313 if itemp \equiv Bz(vc,vt) & vc \equiv 0 1314 if itemp= $Bz(vc, vt) \& vc \neq 0$

1315 if itemp=Load(rd',va) if itemp≡Store(va,v)

 $Proc_p(vt, rf[rd:=op(vI, v2)], clear(bs), im, dm)$

 $Proc_p(pc,rf[rd:=op(vI,v2)],deq(deq(bs)),im,dm)$ $Proc_p(pc,(rf[rd:=op(vI,v2)])[rd':=dm[va]],deq(deq(bs)),im,dm)$

 $\mathsf{Proc}_p(\mathit{pc}, rf[\mathit{rd} := \mathit{op}(\mathit{v1}, \mathit{v2})], \mathsf{deq}(\mathsf{deq}(\mathit{bs})), \mathit{im}, \mathit{dm}[\mathit{va} := \mathit{v}])$

$Proc_p(\rho c, ff, bs, im, dm)$ $if im[pc] \equiv inst and im[pc+1] \equiv inst'$ $and Source(inst) \cap Target(bs) \equiv \emptyset$ $and Source(inst') \cap (Target(bs) \cup Target(inst)) \equiv \emptyset$ $Proc_n((pc+1)+1, ff, eng(eng(bs, Decode(inst)), Decode(inst')), im, dm)$	
1302 1302 1303 1304	

st(bs), itemp:=first(deq(bs))	$\rightarrow \text{Proc}_p(pc,rf[rd:=op(vI,v2)],\text{deq}(\text{deq}(bs)),im,dm)$	Proc _p (vt',rf , clear(\overline{bs}), im,dm)	Proc $_p(pc, rf, \text{deq}(\text{deq}(bs)), im, dm)$	Proc _p ($pc, rf[rd:=dm[va]], deq(deq(bs)), im, dm$)	\rightarrow Proc _p (pc,rf,deq(deq(bs)),im,dm[va:=v])
1321 Proc _p (pc, tt, bs, im, dm) where Bz(vc, vt):=first(bs), itemp:=first(deq(bs))	1322 if itemp= $Op(op,rd,v1,v2)$ & $vc\neq 0$	011		1325 <i>if</i> itemp \equiv Load(rd,va) & vc \neq 0 \rightarrow	1326 if itemp \equiv Store(va,v) & vc \neq 0 \rightarrow

FIG. 13C

 $Proc_p(pc,(rf[rd:=dm[va]])[rd':=\underline{op}(vI,vZ)],deq(deq(bs)),im,dm)$ $Proc_p(vt,(rf[rd:=dm[va]]),clear(bs),im,dm)$ $Proc_o(pc,(rf[rd:=dm[va]]),deq(deq(bs)),im,dm)$ 1331 $Proc_p(pc,rf,bs,im,dm)$ where Load(rd,va):=first(bs), itemp:=first(deq(bs))1 1333 *if itemp* \equiv Bz(vc,vt) & vc \equiv 0 1334 *if itemp*≡Bz(vc,vt) & vc≠0 1332 **if** itemp≡Op(op,rd',v1,v2)

FIG. 13D

 $Proc_p(pc, f[rd:=op(v1,v2)], deq(deq(bs)), im, dm[va:=v]$ $Proc_p(vt, f, clear(bs), im, dm[va:=v])$ $Proc_n(pc.nf.dea(dea(bs)).im.dm[va:=v])$ 1341 $Proc_p(pc, f, bs, im, dm)$ where Store(va, v):=first(bs), itemp:=first(deq(bs))1 1342 *if itemp*≡Op(op,rd,v1,v2)} 1343 *if itemp*≡Bz(vc,vt) & vc≡0 1344 *if itemp*≡Bz(vc,vt) & vc≠0

FIG. 13F